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APPLICATION FOR UNITED STATES PATENT

FOR

MICROELECTRONIC DEVICE SIGNAL TRANSMISSION BY WAY OF A LID

Inventors:

Debendra Mallik
Chris Baldwin
Brent Stone

MICROELECTRONIC DEVICE SIGNAL TRANSMISSION BY WAY OF A LID

BACKGROUND OF THE INVENTION

[0001] Field of the Invention: The present invention relates to apparatus and methods for the transmission of signals to and/or from a microelectronic device. In particular, the present invention relates to delivering signals to and/or from a microelectronic device through a lid.

[0002] State of the Art: Higher performance, lower cost, increased miniaturization of integrated circuit components, and greater packaging densities of integrated circuits are ongoing goals of the computer industry. As these goals are achieved, microelectronic dice become smaller, and, with higher performance, comes an ever increasing number of interconnects, such as pins, lands, and balls, on the active surface of a microelectronic die.

[0003] Microelectronic dice are typically mounted on substrates, called as "interposers", for packaging purposes, as is known to those skilled in the art. An interposer typical comprises a substrate core (e.g., bismaleimide triazine resin, FR4, polyimide materials, and the like) having dielectric layers (e.g., epoxy resin, polyimide, bisbenzocyclobutene, and the like) and conductive traces (e.g., copper, aluminum, and the like) on a top surface thereof to form a top trace network, and dielectric layers and conductive traces on a bottom surface thereof to form a bottom trace network. To achieve electrical interconnect between the top trace network and the bottom trace network, holes are drilled through the substrate core in specific locations and these holes are plated with a conductive material.

[0004] The high interconnect counts on the microelectronic dice requires ever larger and larger interposers. However, interposers are one of the most expensive components of a microelectronic package, and their expensive increases proportionally to its size. Thus, in the

pursuit of lower costs, advancements which reduce the cost of interposers are continually sought by the microelectronic device industry.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

[0006] FIGs. 1a-1c are side cross-sectional views of a fabrication technique for an embodiment of a microelectronic die package, according to the present invention;

[0007] FIG. 2 is a side cross-sectional view of a microelectronic die assembly formed with the microelectronic die package illustrated in FIG. 1c, according to the present invention;

[0008] FIGs. 3a-3c are side cross-sectional views of a fabrication technique for another embodiment of a microelectronic die package, according to the present invention;

[0009] FIG. 4 is a plane view of the heat dissipation assembly, along line 4-4 of FIG. 3b, according to the present invention;

[0010] FIG. 5 is a side cross-sectional view of an embodiment of a microelectronic die package, according to the present invention;

[0011] FIG. 6 is a side cross-sectional view of a microelectronic die assembly formed with the microelectronic die package illustrated in FIG. 3c, according to the present invention;

[0012] FIG. 7 is an oblique view of a hand-held device having a microelectronic assembly of the present integrated therein, according to the present invention; and

[0013] FIG. 8 is an oblique view of a computer system having a microelectronic assembly of the present integrated therein, according to the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

[0014] In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that the various embodiments of the invention, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the invention. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the claims are entitled. In the drawings, like numerals refer to the same or similar functionality throughout the several views.

[0015] The present invention relates to using an electrically conductive lid as a path for conducting signals (preferably power or ground) to and/or from a microelectronic die. Doing such, allows for the delivery of high electrical current driven by higher power and lower voltage and/or fewer conductive traces needed in a substrate and thereby reduces the size and,

thus, the cost of the substrate. Furthermore, as the lid is significantly thicker than the conductive traces on or in the substrate, the invention can provide a low resistance electrical power path to a microelectronic die reducing power distribution on the substrate and reducing DC voltage drop between the microelectronic die and external components, such as a motherboard.

[0016] FIG. 1a illustrates a microelectronic die assembly 100 comprising a microelectronic die 102 (illustrated as a flip chip) physically and electrically attached to an attachment surface 114 of a substrate 104 (such as an interposer, a motherboard, or the like) by a plurality of conductive bumps 106, such as solder balls, conductive particle filled polymers, and the like, extending between pads 108 on an active surface 110 of the microelectronic die 102 and lands 112 on the substrate attachment surface 114. To mechanically and physically reinforce the conductive bumps 106 connecting the microelectronic die pads 108 and the substrate lands 112, an underfill material 116, such as an epoxy material, is disposed therebetween. The microelectronic die 102 may include, but is not limited to central processing units (CPUs), chipsets, memory devices, ASICs, and the like.

[0017] FIG. 1b illustrates a lid assembly 120 comprising a lid 118 and at least one interconnect 122 is disposed proximate an attachment surface 124 of the lid 118. The interconnect 122 may be any electrically conductive material, including but not limited to metal (e.g., lead, tin, silver, copper, aluminum, alloys thereof, etc.) and conductive particle filled polymers. If a metal is used for the interconnect 122, wetting layers (not shown), such gold or the like (as known in the art), may be formed prior to the attachment of the interconnect 122 to assist in attachment thereof. The lid 118 should be constructed from an electrically conductive

material, such as copper (preferred), copper alloys, aluminum, aluminum alloys, and the like. Furthermore, the lid 118 may be an electrically and thermally conductive heat dissipation device, as will be understood to those skilled in the art. The lid 118 is preferably a flat plate having a substantially planar attachment surface 124. Using a flat plate greatly simplifies the fabrication of the lid 118, as compared to complex shapes used in the industry. Additionally, if the lid 118 also functions as a heat dissipation device, a flat plate allows for easily varying the thickness of the lid 118 without significant cost implications, and varying the thickness of the heat dissipating lid 118 allows the management of thermal performance, weight, and overall package thickness depending on application.

[0018] However, it is understood that the lid 118 is not limited to a flat plate. If the lid118 is also a heat dissipation device, it may be of any appropriate shape, including high surface area (e.g., finned) heat sinks, and may include a heat pipe, thermoelectric coolers, and cold plates (refrigeration or liquid cooled), so long as it is electrically conductive.

[0019] A thermal interface material 126 may be disposed on the lid attachment surface 124, preferably in a central portion of the lid attachment surface 124. The thermal interface material 126 should have high thermal conductivity and may include, but is not limited to, thermal grease, phase-change material, metal filled polymer matrix, solder (alloys of lead, tin, indium, silver, copper, and the like), and other such materials known in the art.

[0020] FIG. 1c illustrates the lid assembly 120 of FIG. 1b attached to the microelectronic die assembly 100 of FIG. 1a to form a microelectronic device package 130. The thermal interface material 126 is placed in contact with a back surface 128 of the microelectronic die 102 and, substantially simultaneously, the interconnect 122 is brought into contact with the substrate

attachment surface 114, preferably into contact with at least one interconnect land 132, such as a metal pad, on the substrate attachment surface 114. The interconnect land 132 is connected to a conductive trace (represented by dashed line 134), which is connected to at least one substrate land 112.

[0021] The interconnect land 132 may comprise a reflowable material and the assembly may be heated to reflow the interconnects 122 and/or interconnect lands 132, thereby adhering the interconnects 122 to the substrate attachment surface 114, as well as lid attachment surface 124. Although the interconnects 122 are shown as being spheres, as it is understood that they may be any appropriate shape and, also, the reflow step can deform the shape of the resulting interconnects.

[0022] It is, of course, understood that the thermal interface material 126 could be disposed on the microelectronic die back surface 128, rather than on the lid attachment surface 124, and/or the plurality of interconnects 122 could be disposed on the substrate attachment surface 114, rather than on the lid attachment surface 124, prior to the attachment of the lid 118.

[0023] At least one electronic line provides an electronic signal (i.e., power, ground, and I/O signal) to the lid 118. The electronic line (shown as dashed line 136) may be attached directly to the lid 118. Thus, as shown in FIG. 1c, the signal may be delivered to the microelectronic die 102 by way of the interconnect 122, the interconnect land 132, the conductive trace 134, the substrate land 112, the conductive bump 106, and the microelectronic die pad 108. Furthermore, as shown in FIG. 1c, the electronic line (shown as dashed line 138) may be within or on the substrate 104 and connected to at least one interconnect 122, thereby providing an electronic signal path to the lid 118. The lid may then be used to distribute the electronic signal, as

previously discussed. It is, of course, understood that every interconnect 122 connected to the lid 118 will transmit (or receive) the same electronic signal.

[0024] The microelectronic device package 130 of FIG. 1c may be incorporated into a socket 142 as shown in FIG. 2 to form a socketed microelectronic device assembly 140. The socket 142 comprises a first surface 144 and an opposing second surface 146 with a recess 148 formed therein extending from the socket first surface 144. The substrate 104 and microelectronic die 102 are disposed in the socket recess 148 with the lid attachment surface 124 proximate the socket first surface 144. The socket second surface 146 has a plurality of external contacts 152 attached thereto. These external contacts 152 generally make contact with an external device (not shown), such as a motherboard.

[0025] The socket 142 includes at least on one first signal line 154 contacting at least one external contact 152, extending through the socket 142 from the socket second surface 146 to the socket first surface 144, and contacting the lid 118. Thus, a signal may delivered through the first signal line 154 to the lid 118, then from the lid 118 to the microelectronic die 102 in a manner previously described.

[0026] The socket 142 may further include at least one second signal line 162 contacting at least one external contact 152, extending through the socket 142 from the socket second surface 146 to a bottom 164 of the socket recess 148, and contacting a second surface 166 of the substrate 104. It is, of course, understood that the first signal line 154 and the second signal line 162 may comprise a combination of conductive elements and may take a circuitous route through the socket 142, rather than the illustrated straight signal lines, as will understood by those skilled in the art.

[0027] As will be understood by those skilled in the art, the substrate 104 may include a substrate core (e.g., bismaleimide triazine resin, FR4, polyimide materials, and the like) having dielectric layers (e.g., epoxy resin, polyimide, bisbenzocyclobutene, and the like) and conductive traces (e.g., copper, aluminum, and the like) on a top surface thereof to form a top trace network, and dielectric layers and conductive traces on a bottom surface thereof to form a bottom trace network. To achieve electrical interconnect between the top trace network and the bottom trace network, holes are drilled through the substrate core in specific locations and these holes are plated with a conductive material. The resulting plated holes are known in the art as "plated through-hole (PTH)" vias. Thus, an electronic signal may be delivered and/or received through the second signal line 162, through the substrate 104, and to the microelectronic die 102 by way of the substrate lands 112, conductive bumps 106, and microelectronic die pads 108. Additionally, passive devices 168, such as capacitors, resistors, and the like may be attached to the substrate second surface 166.

[0028] FIG. 3a illustrates another microelectronic die assembly 200 according to the present invention comprising a microelectronic die 202 (illustrated as a flip chip) physically and electrically attached to an attachment surface 214 of a substrate 204 (such as an interposer, a motherboard, or the like) by a plurality of conductive bumps 206, such as solder balls, conductive particle filled polymers, and the like, extending between pads 208 on an active surface 210 of the microelectronic die 202 and lands 212 on the substrate attachment surface 214. To mechanically and physically reinforce the conductive bumps 206 connecting the microelectronic die pads 208 and the substrate lands 212, an underfill material 216, such as an epoxy material, is disposed therebetween. The microelectronic die 202 may include, but is not limited to central processing units (CPUs), chipsets, memory devices, ASICs, and the like.

[0029] FIG. 3b illustrates a lid assembly 220 comprising a lid 218, at least one first interconnect 222 disposed on and in electrical contact with an attachment surface 224 of the lid 218, and at least one second interconnect 226 disposed proximate, but electrically isolated from an attachment surface 224 of the lid 218. The second interconnects 226 are electrically isolated by a dielectric layer 228 disposed on the lid attachment surface 224. An electrically conductive signal trace 232 is disposed on the dielectric layer 228 and the second interconnect 226 is attached to the conductive signal trace 232. The lid attachment surface 224 may have height variations 230 thereon such that the first interconnects 222 and the second interconnects 226 may be substantially the same size in size or height.

[0030] The first interconnect 222 and the second interconnect 226 may be any electrically conductive material, including but not limited to metal (e.g., lead, tin, silver, copper, aluminum, alloys thereof, etc.) and conductive particle filled polymers. If a metal is used for the first interconnect 222 and/or the second interconnect 226, wetting layers (not shown), such gold or the like (as known in the art), may be formed prior to the attachment of the first interconnect 222 and/or second interconnect 226 to assist in attachment thereof. The lid 218 should be constructed from a thermally conductive and electrically conductive material, such as copper, copper alloys, aluminum, aluminum alloys, and the like.

[0031] A thermal interface material 234 may be disposed on the lid attachment surface 224, preferably in a central portion of the lid attachment surface 224. The thermal interface material 234 should have high thermal conductivity and may include, but is not limited to, thermal grease, phase-change material, metal filled polymer matrix, solder (alloys of lead, tin, indium, silver, copper, and the like), and other such materials known in the art.

[0032] FIG. 3c illustrates the heat dissipation assembly 220 of FIG. 3b attached to the microelectronic die assembly 200 of FIG. 3a to form a microelectronic device package 240. The thermal interface material 234 is placed in contact with a back surface 242 of the microelectronic die 202 and, substantially simultaneously, the first interconnect 222 is brought into contact with the substrate attachment surface 214, preferably into contact with at least one first interconnect land 244, such as a metal pad, on the substrate attachment surface 214 and the second interconnect 226 is brought into contact with the substrate attachment surface 214, preferably into contact with at least one second interconnect land 246, such as a metal pad, on the substrate attachment surface 214. The first interconnect land 244 is connected to a first conductive trace (represented by dashed line 252), which is connected to at least one substrate land 212. The second interconnect 226 is connected to a second conductive trace (represented by dashed line 254), which is connected to at least one substrate land 212.

[0033] The first interconnect land 244 and second interconnect land 246 may comprise a reflowable material and the assembly may be heated to reflow the first interconnects 222 and second interconnects 226 and/or the first interconnect lands 244 and second interconnect lands 246, thereby adhering the first interconnects 222 to the substrate attachment surface 214, as well as the lid attachment surface 224 and adhering the second interconnects 226 to the conductive signal traces 232.

[0034] At least one electronic line provides a first electronic signal (i.e., power, ground, and I/O signal) to the lid 218. The electronic line (shown as dashed line 256) may be attached directly to the lid 218. Thus, as shown in FIG. 3c, the first electronic signal may be delivered to the microelectronic die 202 by way of the first interconnect 222, the first interconnect land 244, the first conductive trace 252, the substrate land 212, the conductive bump 206, and the

microelectronic die pad 208. It is, of course, understood that every first interconnect 222 connected to the lid 218 will transmit (or receive) the same electronic signal.

[0035] Furthermore, as shown in FIG. 3c, at least one electronic line provides a second electronic signal (i.e., power, ground, and I/O signal) to the conductive signal trace 232. An electronic line (shown as dashed line 258) may directly connect to the conductive signal trace 232, thereby proving the signal to the microelectronic die 202 by way of the second interconnect 226, the second interconnect land 246, the second conductive trace 254, the substrate land 212, the conductive bump 206, and the microelectronic die pad 208. As shown in FIG. 4, the conductive signal trace 232 may contact all of the second interconnects 226, thereby providing the same signal to all. Of course, it is understood that the invention includes any number of conductive signal traces 232 having differing discrete signals delivered to or received therefrom. It is, of course, understood that the conductive signal trace(s) 232 could be the only conductive element(s) of the lid (i.e., the lid being an insulative lid 236 and all signal being delivered with conductive signal traces 232), as shown in FIG. 5.

[0036] The microelectronic die package 240 of FIG. 3c may be incorporated into a socket 262 as shown in FIG. 5 to form a socketed microelectronic device package 260. The socket 262 comprises a first surface 264 and an opposing second surface 266 with a recess 268 formed therein extending from the socket first surface 264. The substrate 204 and microelectronic die 202 are disposed in the socket recess 268 with the lid 218 proximate the socket first surface 264. The socket second surface 266 has a plurality of external contacts 272 attached thereto. These external contacts 272 generally make contact with an external device (not shown), such as a motherboard.

[0037] The socket 262 includes at least on one first signal line 274 contacting at least one external contact 272, extending through the socket 262 from the socket second surface 266 to the socket first surface 264, and contacting the lid 218. Thus, a signal may delivered through the first signal line 274 to the lid 218, then from the lid 218 to the microelectronic die 202 in a manner previously described. The socket 262 may further include at least one second signal line 282 contacting at least one external contact 272, extending through the socket 262 from the socket second surface 266 to a bottom 284 of the socket recess 268, and contacting a second surface 286 of the substrate 204.

[0038] The socket 262 also includes at least on one third signal line 292 contacting at least one external contact 272, extending through the socket 262 from the socket second surface 266 to the socket first surface 264, and contacting the conductive signal trace 232. Thus, a signal may delivered through the third signal line 292 to the conductive signal trace 232, then from the conductive signal trace 232 to the microelectronic die 202 in a manner previously described. It is, of course, understood that the first signal line 274, the second signal line 282, and the third signal line 292 may comprise a combination of conductive elements and may take a circuitous route through the socket 262, rather than the illustrated straight signal lines, as will understood by those skilled in the art.

[0039] The packages formed by the present invention may be used in a hand-held device 310, such as a cell phone or a personal data assistant (PDA), as shown in FIG. 6. The hand-held device 310 may comprise an external substrate 320 with at least one of the microelectronic device package 130 of FIG. 1c, the socketed microelectronic device package 140 of FIG. 2, the microelectronic device package 240 of FIG. 3c, and the socketed microelectronic device package 260 of FIG. 5 collectively represented as element 330 attached thereto, within a housing 340.

The external substrate 320 may be attached to various peripheral devices including an input device, such as keypad 350, and a display device, such an LCD display 360.

[0040] The microelectronic device assemblies formed by the present invention may also be used in a computer system 410, as shown in FIG. 7. The computer system 410 may comprise an external substrate or motherboard 420 with at least one of the microelectronic device package 130 of FIG. 1c, the socketed microelectronic device package 140 of FIG. 2, the microelectronic device package 240 of FIG. 3c, and the socketed microelectronic device package 260 of FIG. 5 collectively represented as element 430 attached thereto, within a housing or chassis 440. The external substrate or motherboard 420 may be attached to various peripheral devices including inputs devices, such as a keyboard 450 and/or a mouse 460, and a display device, such as a CRT monitor 470.

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[0041] Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.